PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
Albihns Stockholm AB
P O Box 5581
114 85 STOCKHOLM

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)* 30-04-2004

Applicant's or agent's file reference
74137

FOR FURTHER ACTION
See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/SE2004/000103	27-01-2004	28-01-2003

International Patent Classification (IPC) or both national classification and IPC
G06F 9/38

Applicant
Xelerated AB et al

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further opinions, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/SE
Patent- och registreringsverket
Box 5055
S-102 42 STOCKHOLM
Facsimile No. +46 8 667 72 88

Authorized officer
Pär Heimdal /LR
Telephone No. +46 8 782 25 00

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/SE2004/000103

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This opinion has been established on the basis of a translation from the original language into the following language _____, which is the language of a translation furnished for the purposes of international search (under Rules 12.3 and 23.1(b)).

2. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application and necessary to the claimed invention, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ in written format

      ☐ in computer readable form

   c. time of filing/furnishing

      ☐ contained in the international application as filed.

      ☐ filed together with the international application in computer readable form.

      ☐ furnished subsequently to this Authority for the purposes of search.

3. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

4. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/SE2004/000103

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	5-9	YES
	Claims	1-4	NO
Inventive step (IS)	Claims		YES
	Claims	1-9	NO
Industrial applicability (IA)	Claims	1-9	YES
	Claims		NO

2. Citations and explanations:

CITATIONS
The examination process has revealed the following documents:

D1: US20020054594 A1
D2: AHUJA et al. 'Multipath Execution: Opportunities and Limits'. Conference Proceedings of the 1998 International Conference on Supercomputing. Melbourne, Vic., Australia, 13-17 July 1998. ISBN 0-89791-998-X, sid 101-108.
D3: LEE, 'Programmable DSP Architectures: Part II'. IEEE ASSP Magazine, Vol. 6, issue 1, January 1989. ISSN: 0740-7467, sid 4-14.
D4: Eklund, 'Modern mikroprocessordesign - med introduktion till parallella datorsystem'. Studentlitteratur, Lund, 1999. ISBN 91-44-01225-X, sid 133.

STATEMENT
Document D1, which is considered to represent the most relevant prior art, presents a method for increasing the velocity at a processor when processing data packets. The processor includes a number of logical blocks, called pipeline stages. In each stage, operations are performed on a packet, and the packet is propagated to the next stage, see [0008]. It appears evident from figure 7 and [0022, 0043-0045] that each pipeline stage in itself is pipelined, so that a new instruction could start executing before the latest instruction is finished. The novel instruction could belong to the same packet as the earlier, but could also be associated with another packet.

.../...

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box V

In order to make the next pipeline stage continue the processing of the packet, certain information must be sent from the preceding stage. In [0024] is described how the processor creates a frame context for each packet, where packet data and related information, such as register content, is saved.

This frame context is sent further to the next stage for further processing, see [0025]. Even if it is not explicitly described in D1 that calculations could be saved in a frame context, that is considered obvious to a person skilled in the art to do so. It is mentioned that register content must be saved, which implicate that partial calculation results are transferred. It would also be impossible for the next stage to continue to execute, if the earlier results where not transferred. Thus a frame context in D1 appears to correspond to the expression context in your application.

Document D2 describes technological advances in order to minimize time loss when mispredicting branches in a pipelined processor. Instead of guessing which branch that will be taken, all possible branches are executed simultaneously. When it is clear which branch is the correct one, the other executions are thrown, see page 1.

Document D3 describes different methods for making pipelined systems easier to program. If the programmer must know how all instructions are pipelined, the programming becomes much more complex. An example of how this could be solved is through interlocking, see paragraph 2.1, where the pipeline stage are covered and the programmer could assume that one instruction always has terminated before the next one begins.

Document D4 describes so called forwarding, or bypassing.

Claims 1 and 2:
The invention as defined by claims 1 and 2 are previously known from D1, see figure 7 and [0024]. Thus claim 1 and 2 lacks novelty.

.../...

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box V

Claims 3 and 4:
In D1 is described how the first pipeline stage performs a partial operation included in an instruction belonging to a first packet, see [0011]. The instruction is then forwarded to the next stage, performing the following partial operation, at the same time as the first stage performs an operation on a new packet. It is thus described in D1 that an operation is divided in a plurality of partial operations and that the partial operations could be performed in different pipeline stages.

In claim 3 is described that a first partial operation belonging to a context is performed in a first stage. Thereafter, the context is sent further to the next stage where a second partial operation is performed. Simultaneously (also in the second stage) is the first partial operation for the next operation performed. That corresponds to a combination of what is described in figure 7 and in paragraph [0011] in D1. According to paragraph [0011], a first partial operation on an instruction in stage one, then the context, including the instruction is sent further to stage two. In stage two, the second partial operation starts on the same instruction. It does not appear from [0011] that something occurs at the same time in step two. It is however clear from figure 7. Each stage has an internal pipelining, so that when the second partial operation starts in stage two, the pipeline will be filled with a new partial operation for a new instruction. The new instruction could concern the same context, see line 2-3 in the diagram in figure 4.

In claim 4 is also stated that a new operation on a new context is started to be done in stage one before the second

Partial operation is completed in stage two. So is done also in D1, see the two last sentences in paragraph [0011].

Thus the invention according to claims 3-4 lacks novelty.

.../...

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box V

Claim 5:
As said before, it is considered obvious to let partial results from earlier operations be included in a frame context, otherwise the system according to D1 could not work according to the description. What is described in claim 5 thus lacks an inventive step.

Claims 6-7:
The invention according to claims 6-7 differs from the art in D1 in that alternative ways of execution are handled differently. According to the claims, all alternative ways are performed and the different partial results are saved. Then is decided which way that was the correct one and the partial result from that branch is used in the further processing.

In D1 the problem was instead solved by changing to another context when a possible stall of the pipeline is detected in one of the stages, see paragraph [0027].

A person skilled in the art, with knowledge of D1, thus stands before the problem of finding alternative solutions to manage alternative ways of execution faster. The solution in D1 means that the first context not will be treated before the conflict is solved, and the person skilled in the art could be expected to search for solutions making it possible to directly continue with the operations of the first context, in order to achieve a system where the maximized time of execution of a packet is reduced.

The person skilled in the art should thus search among known solutions to this problem and find document D2.

In D2 the person skilled in the art find that all alternative ways of execution is performed simultaneously. By modifying the system in D1 with features from D2, the person skilled in the art will reach the system according to claims 6-7.

The invention according to claims 6-7 consequently lacks an inventive step.

.../...

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of: Box V

Claim 8:
The invention according to claim 8 differs from document D1 in that the second partial operation for an instruction is presented to the programmer as if it was performed in stage one, even if it is performed in stage two.

The formulated problem, that pipelining makes the system more difficult to program is well known in the art of computer science. A previously known solution to this problem is to let the programmer assume that an operation has been completed in an earlier stage, see document D3.

The invention defined by claim 8 is thus not considered to involve an inventive step.

Claim 9:
Claim 9 differs from D1 in that so called forwarding is used, meaning that an operand is fetched directl from an earlier instruction instead of from a register. Forwarding is well known in the art of pipelining, see e.g. D4, page 133. It appears obvious to a person skilled in the art that the necessary partial results are sent in the context.

The invention defined by claim 9 is thus not considered to involve an inventive step.